What is claimed is:

1. A method comprising:

translating a design description into configurations for a plurality of processing elements, wherein a plurality of functions in the design description are implemented on one of the plurality of processing elements; and

setting at least one output packet size corresponding to at least one of the plurality of functions.

2. The method of claim 1 wherein setting at least one output packet size comprises setting independent output packet sizes for more than one of the plurality of functions.

3. The method of claim 1 wherein setting at least one output packet size comprises setting an independent output packet size for each of the plurality of functions.

4. The method of claim 3 further comprising estimating network performance.

5. The method of claim 4 further comprising modifying the at least one output packet size and re-estimating network performance.

6. The method of claim 1 wherein translating comprises compiling the plurality of functions to code to run on the one of the plurality of processing elements.

7. The method of claim 1 wherein setting a packet size comprises dividing a function output block size into smaller physical block sizes.

8. The method of claim 7 wherein setting a packet size further includes adding a packet header size to the physical block size.

9. The method of claim 1 further comprising profiling a design represented by the configurations for the plurality of processing elements.

10. The method of claim 9 further comprising changing the at least one output packet size in response to the profiling.

11. The method of claim 9 further comprising comparing user constraints with output from the profiling.

12. The method of claim 11 wherein the user constraints include latency.

13. The method of claim 11 wherein the user constraints include throughput.

14. The method of claim 1 wherein each of the plurality of functions has an output block size, and wherein setting at least one output packet size comprises dividing the output block size to set a physical packet size.

15. The method of claim 14 wherein setting at least one output packet size further comprises estimating network performance.

16. The method of claim 15 further comprising changing the physical packet size in response to the estimating.

17. The method of claim 15 wherein profiling produces information describing throughput.

18. A method comprising:

dividing a design description into a plurality of functions;

mapping at least two of the plurality of functions onto one of a plurality of processing elements in an integrated circuit;

setting a first output packet size for a first of the at least two of the plurality of functions; and

setting a second output packet size for a second of the at least two of the plurality of functions.

19. The method of claim 18 wherein the first of the at least two of the plurality of functions has an output block size, and wherein the first output packet size is smaller than the output block size.

20. The method of claim 18 further comprising generating configuration packets to configure the integrated circuit.

21. The method of claim 20 further comprising configuring the integrated circuit with the configuration packets.

22. The method of claim 20 further comprising profiling a design with the configuration packets.

23. The method of claim 22 further comprising modifying the first output packet size in response to the profiling.

24. An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

reading a design description;

compiling the design description to configure a plurality of processing elements, wherein a plurality of functions in the design description are mapped to one of the plurality of processing elements; and

independently determining output packet sizes for each of the plurality of functions.

25. The apparatus of claim 24 wherein the machine-accessible instructions when accessed further result in the machine performing:

estimating a performance of the plurality of processing elements; and

modifying at least one of the output packet sizes in response to the estimating.

26. The apparatus of claim 25 wherein estimating a performance comprises determining if throughput constraints are met.

27. The apparatus of claim 26 wherein determining if throughput constraints are met comprises determining if throughput constraints for each of the plurality of functions are met.

28. An electronic system comprising:

a processor; and

a static random access memory to hold instructions that when accessed result in the processor performing translating a design description into configurations for a plurality of processing elements on a single integrated circuit, wherein a plurality of functions in the design description are implemented on one of the plurality of processing elements, and setting at least one output packet size corresponding to at least one of the plurality of functions.

29. The electronic system of claim 28 wherein setting at least one output packet size comprises setting independent output packet sizes for more than one of the plurality of functions.

30. The electronic system of claim 29 wherein setting at least one output packet size comprises setting an independent output packet size for each of the plurality of functions.